REMARKS/ARGUMENTS

Favorable consideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-49, 51-57, 67, 68, 71-76 and 79-112 are presently pending in this application, Claims 50, 58-66, 69, 70, 77 and 78 having been canceled, Claims 1, 3-7, 10-13, 15-17, 21, 23-26, 28-30, 34, 36-40, 46, 48, 49, 51-54, 56, 57, 67, 68, 71-76, 79-81, 85-87, 89 and 90 having been amended and Claims 93-112 having been newly added by the present amendment.

In the outstanding Office Action, the application was objected to under CFR 1.172(a) as lacking the written consent of all assignees; Claims 77 and 78 were rejected under 35 U.S.C. §112, second paragraph, for being indefinite; Claims 1-20, 23-26, 28-33, 36-42, 48, 52-55, 58, 66, 68, 87, 88 and 92 were rejected under 35 U.S.C. §102(b) as being anticipated by Nakatani et al. (U.S. Patent 5,484,647); Claims 1-20, 23-26, 28-33, 36-42, 48, 52-55, 58, 66, 68, 72, 81-83, 87, 88 and 92 were rejected under 35 U.S.C. §102(b) as being anticipated by Hatakeyama et al. (U.S. Patent 5,972,482);Claims 1, 2, 4, 5, 7, 8, 11-13, 16, 17, 19-21, 24, 25, 29, 30-33, 37-42, 46-67, 87, 88 and 92 were rejected under 35 U.S.C. §102(b) as being anticipated by Yasue et al. (U.S. Patent 6,010,768,); Claims 1-92 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yasue et al. or Nakatani et al. or Hatakeyama et al.; and Claims 1-92 were rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over Claims 1-55 of U.S. Patent 6,376,052.

In response to the objection under CFR 1.172(a), submitted herewith, as requested by the Examiner, is a copy of the written consent of the assignee of the original patent, the statement under 37 CFR 3.73(b) and assignment, which were filed on July 26, 2004, as evidenced by a copy of the date-stamped filing receipt. These submissions are believed to satisfy the requirements under 37 CFR 1.172(a) and 3.73(b). If, however, the Examiner

disagrees, the Examiner is invited to telephone the undersigned who will be happy to supplement the present submission.

Claims 1, 3-7, 10-13, 15-17, 21, 23-26, 28-30, 34, 36-40, 46, 48, 49, 51-54, 56, 57, 67, 68, 71-76, 79-81, 85-87, 89 and 90 having been amended and Claims 93-112 having been newly added herein. Regarding Claims 87, 89 and 90, Claims 87, 89 and 90 have been amended as follows:

87. A multilayer printed wiring board comprising:

a substrate having ~~at least one~~ a through-hole structure ~~which includes a roughened internal surface~~ comprising a plating layer and a filler provided in the through-hole structure, the plating layer having a roughened portion;

a first conductor layer having a first conductor circuit formed on the substrate and a through-hole-covering conductor layer covering the filler provided in contact with the plating layer;

~~at least one~~ a first interlaminar resin insulating layer ~~which is provided on the substrate and in which at least one~~ having a via hole ~~is provided~~ and being formed on the substrate and the first conductor layer; and

a second conductor layer having ~~at least one~~ a second conductor circuit ~~provided~~ formed on the first interlaminar resin insulating layer, the second conductor circuit being connected to the first conductor circuit by the via hole~~;~~

~~filler provided in the through-hole; and~~

~~a through-hole-covering conductor layer provided to cover the filler provided in the through-hole, said at least one via hole being connected to said through-hole-covering conductor layer~~.

89. The multilayer printed wiring board according to Claim 87, wherein ~~a roughened layer is provided on~~ a surface of said through-hole-covering conductor layer is roughened.

90. The multilayer printed wiring board according to Claim 89, wherein ~~the roughened layer is provided on~~ a side face of said through-hole-covering conductor layer is roughened.

These claim amendments and additions are believed to be clearly supported by the original patent, for example, column 9, lines 47-49 and 58-61, column 17, line 36 to column 18, line 40, column 24, lines 49-58, and Figs. 2(a)-4(d). Therefore, no new matter is believed to be added. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work in a joint effort to derive mutually satisfactory claim language. Also, Applicants respectfully request that Claims 50, 58-66, 69, 70, 77 and 78 be canceled without prejudice.

Furthermore, in response to the rejection based on the obviousness-type double patenting, submitted herewith is a Terminal Disclaimer to overcome the rejection based on Claims 1-55 of U.S. Patent 6,376,052. Applicants therefore respectfully request that the obviousness-type double patenting rejection be withdrawn.

Briefly recapitulating, Claim 1 as currently amended is directed to a multilayer printed wiring board including a substrate having one or more through-hole structures, one or more interlaminar resin insulating layers formed on the substrate, and one or more conductor circuits formed on the interlaminar resin insulating layer. The through-hole structure is comprised of a plated film and filled with filler, a surface of the plated film of the through-hole structure is roughened, and the filler is comprised of metal particles and either thermosetting or thermoplastic resin. By providing such a through-hole structure, the conductor resistivity is sufficiently reduced in the printed wiring board of Claim 1.

Furthermore, since the filler contains metal particles, the filler and the plated film in the through-hole structure are more firmly adhered to each other.

Yasue et al. is related to a multilayer printed circuit board. Nevertheless, Yasue et al. does not teach "a substrate having at least one through-hole structure, the at least one through-hole structure comprising a plated film and being filled with filler; ... wherein ... the filler comprises metal particles and one of thermosetting and thermoplastic resin" as recited in amended Claim 1. On the other hand, Yasue et al. merely describes a multilayer printed circuit board having a through-hole filled with a filler including a resin component, curing agent and inorganic particles,[1] but not including metal particles, as pointed out in the Office Action, page 7. Thus, Claim 1 is believed to be clearly distinguishable from Yasue et al.

Nakatani et al. and Hatakeyama et al. also discuss printed circuit boards, but fail to teach the substrate as recited in amended Claim 1. Specifically, Nakatani et al. simply describes a substrate which is made of porous base material 102 and has through-holes 103 filled with conductive paste 104.[2] Similarly, Hatakeyama et al. only discusses a printed circuit board 610 having voids 607 and a through-hole filled with a conductive paste 603.[3] Since these substrates of Nakatani et al. and Hatakeyama et al. include voids, there are possibilities that the voids thermally expand to cause cracking and that moisture in the voids deteriorates insulation resistance. On the other hand, in the substrate as recited in Claim 1, since the through-hole structure has the plated film, excellent adhesion is achieved between the filler and the plated film. Claim 1 is therefore believed to be clearly distinguishable from Nakatani et al. and Hatakeyama et al.

Because none of Yasue et al., Nakatani et al. and Hatakeyama et al. discloses the substrate as recited in Claim 1, even the combined teachings of these cited references are not

[1] See Yasue et al., column 12, lines 45-48.
[2] See Nakatani et al., column 13, line 61, to column 14, line 11.
[3] See Hatakeyama et al., column 12, lines 36-48.

believed to render the structure recited in Claim 1 obvious. In particular, the conductive paste described in Nakatani et al. and Hatakeyama et al. is filled in the through-hole so as to provide electrical connection in the thickness direction of the substrate. On the other hand, in the Yasue et al. device, the electrical connection in the thickness direction is established in the through-hole. Therefore, the conductive paste of Nakatani et al. and Hatakeyama et al. is not believed to be applicable to the Yasue et al. structure.

Turning to Claim 5, Claim 5 as currently amended is directed to a multilayer printed wiring board including a substrate having one or more through-hole structures, one or more interlaminar resin insulating layers formed on the substrate, and one or more conductor circuits formed on the interlaminar resin insulating layer. The through-hole structure is filled with filler, an internal surface of the through-hole structure is roughened, and the filler is comprised of particulate substance including metal particles having a particle size of from 0.1 to 30 μm, resin, and ultrafine inorganic powder having a particle size from 2 to 100 nm. By having a substrate with such a through-hole structure, the printed wiring board has less malfunctions because the filler in the through-hole structure is more uniformly filled with less sedimentation.

Nakatani et al., Hatakeyama et al. and Yasue et al. are all related to printed circuit boards, but none of these references teaches "a substrate having at least one through-hole structure, the at least one through-hole structure being filled with filler; ... wherein ... the filler comprises particulate substance including metal particles having a particle size of from 0.1 to 30 μm, resin, and ultrafine inorganic powder having a particle size from 2 to 100 nm" as recited in amended Claim 5. On the other hand, Nakatani et al. discusses a conductive paste including a metallic filler and states that "[i]n order to disperse the conductive fillers with high concentration, an average particle size of the conductive filler should be preferably

from 0.2 to 20 μm, and should also have as small specific surface as possible."[4] As such, Nakatani et al. is believed to teach away from the use of ultrafine inorganic powder having a smaller particle size and larger specific surface as in Claim 5. Hatakeyama et al. also discusses a conductive paste having metal particles having an average diameter of from 0.2 to 20 μm, and further suggests that the particle size range is preferably from 50 to 300 μm "to maintain high electrical conductivity."[5] Therefore, like Nakatani et al., Hatakeyama et al. is believed to teach away from the claimed filler including ultrafine inorganic powder. Yasue et al. merely describes a resin filler which does not contain metal particles. For the foregoing reasons, the structure of Claim 5 is believed to be clearly distinguishable from Nakatani et al., Hatakeyama et al. and Yasue et al.

Next, Claim 17 as currently amended is directed to a multilayer printed wiring board including a substrate having one or more through-hole structures, one or more interlaminar resin insulating layers formed on the substrate and one or more conductor circuits formed on the interlaminar resin insulating layer. The through-hole structure is filled with filler, an internal surface of the through-hole structure is roughened, the filler is comprised of particulate substance having a particle size of from 0.1 to 30 μm, resin, and ultrafine inorganic powder having a particle size from 2 to 100 nm, and an exposed portion of the filler in the through-hole structure is covered with a through-hole-covering conductor layer. By having such a substrate, the printed wiring board can have a via hole at a position directly above the through-hole structure and is more desirable for making fine circuit patterns.

On the other hand, Nakatani et al., Hatakeyama et al. and Yasue et al. fail to teach "a substrate having at least one through-hole structure, the at least one through-hole structure being filled with filler; ... wherein ... the filler comprises particulate substance having a

[4] Nakatani et al., column 9, lines 36-40.
[5] Hatakeyama et al., column 5, lines 47-50.

particle size of from 0.1 to 30 μm, resin, and ultrafine inorganic powder having a particle size from 2 to 100 nm, and an exposed portion of the filler in the at least one through-hole structure is covered with a through-hole-covering conductor layer" recited in amended Claim 17. As discussed above, both Nakatani et al. and Hatakeyama et al. simply describe a conductive paste having metal particles with a larger particle size than the ultrafine inorganic powder as recited in Claim 17. Yasue et al. only discusses a through-hole structure covered by an insulating material 2 as illustrated in Fig. 3E. Hence, the structure recited in Claim 17 is believed to be distinguishable from Nakatani et al., Hatakeyama et al. and Yasue et al.

Turning now to Claim 87, Claim 87 as currently amended is directed to a multilayer printed wiring board including a substrate, a first conductor layer, a first interlaminar resin insulating layer and a second conductor layer. The substrate has a through-hole structure including a plating layer and a filler provided in the through-hole structure, and the plating layer has a roughened portion. The first conductor layer has a first conductor circuit formed on the substrate and a through-hole-covering conductor layer covering the filler provided in the through-hole structure having the plating layer. The first interlaminar resin insulating layer has a via hole and is formed on the substrate and the first conductor layer. The second conductor layer has a second conductor circuit formed on the first interlaminar resin insulating layer, and the second conductor circuit is connected to the first conductor circuit by the via hole. By having the first conductor layer having such a through-hole-covering conductor layer, the printed wiring board allows formation of a via hole directly above the through-hole structure which is advantage for having fine circuit patterns.

On the other hand, none of Nakatani et al., Hatakeyama et al. and Yasue et al. teaches "a first conductor layer having a first conductor circuit formed on the substrate and a through-hole-covering conductor layer covering the filler provided in the through-hole structure having the plating layer" recited in Claim 87 as currently amended. Specifically, Nakatani et

al. and Hatakeyama et al. simply describes substrates having through-holes filled with a conductive paste, and Yasue et al. merely discusses a substrate having a through-hole covered by an insulating layer. The structure of Claim 87 is thus believed to be distinguishable from Nakatani et al., Hatakeyama et al. and Yasue et al.

For the foregoing reasons, Claims 1, 5, 12, 17 and 87 are believed to be allowable. Also, independent Claim 25 is directed to a multilayer printed wiring board and recites "a substrate having at least one through-hole structure comprising a plated film and being filled with filler; ... wherein ... the filler comprises metal particles and one of thermosetting and thermoplastic resin, an exposed surface of the filler in the at least one through-hole structure is covered with a through-hole-covering conductor layer," Claim 30 is directed to a multilayer printed wiring board and recites "a substrate having at least one through-hole structure, the at least one through-hole structure being filled with filler; ... wherein ... the filler comprises ... ultrafine inorganic powder having a particle size from 2 to 100 nm, and an exposed surface of the filler in the at least one through-hole structure is covered with a through-hole-covering conductor layer," Claim 38 is directed to a resin composition for filling through-hole of a printing wiring board and recites "particulate substance comprising metal powder having an average particle size ranging from 0.1 to 30 μm ... and ultrafine inorganic powder having an average particle size ranging from 2 to 100 nm," Claim 48 is directed to a process of producing a multilayer printed wiring board and recites "filling the through-hole structure including the plated layer having a roughened surface with filler comprising metal particles and one of thermosetting and thermoplastic resin," Claim 52 is directed to a process of producing a multilayer printed wiring board, and recites "filling the through-hole structure including the plated layer having a roughened surface with filler comprising ... ultrafine inorganic powder having a particle size from 2 to 100 nm," Claim 72 is directed to a process of producing a multilayer printed wiring board and recites "filling the

through-hole structure including the plated layer having a roughened surface with filler comprising metal particles and one of the thermosetting and thermoplastic resin," Claim 81 is directed to a process of producing a multilayer printed wiring board and recites "filling the through-hole structure including the plated layer having a roughened surface with filler comprising particulate substance having a particle size of from 0.1 to 30 μm, resin, and ultrafine inorganic powder having a particle size from 2 to 100 nm," and Claim 110 is directed to a process of producing a multilayer printed wiring board and recites "forming a through-hole structure in the substrate, the forming including plating a layer on a surface of the hole; ... forming a first conductor layer having a first conductor circuit on the substrate and a through-hole-covering conductor layer covering the filler by plating." As such, substantially the same arguments are believed to be applicable to independent Claims 25, 30, 38, 48, 52, 72, 81 and 110 and the rest of the dependent claims. Therefore, Claims 1-49, 51-57, 67, 68, 71-76 and 79-112 are all believed to be allowable.

In view of the amendments and discussions presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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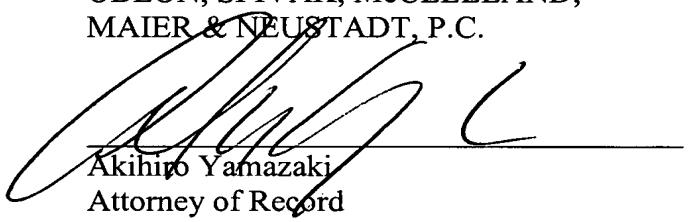

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